Arnav Nevgi

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SUMMARY

Final-year B.Tech Electrical and Electronics student targeting entry-level **ASIC Verification, RTL Design and FPGA roles**; open to **U.S. relocation**. Built GitHub-documented **SystemVerilog** projects in AXI4 verification, cache ECC MBIST RTL, UART FPGA implementation, SVA, scoreboards, coverage and timing closure, with **1+ year of internship experience** in digital interface debugging and HW-SW integration.

PROFESSIONAL EXPERIENCE

Indian Institute of Science, Centre of Data for Public Good *Jan 2026 – Jun 2026*

Electrical Research Intern *Bangalore, India*

- Designed a secure inter-cloud pipeline using **OIDC**, AWS STS, AWS KMS, envelope encryption and **TEE computing**.
- Developed and debugged **TEE-attestation validation flows**, completing **85%+ of planned validation scenarios** across enclave startup, encrypted handoff, boot-state reporting, JWT/OIDC exchange, EC-key validation, trust-boundary checks and policy validation.

Ceremorphic Technologies Private Limited *Aug 2025 – Oct 2025*

Embedded Systems and Algorithm Intern *Hyderabad, India*

- Contributed to secure bootloader development for a **Caliptra-inspired HPC SoC platform**, supporting trusted boot, firmware authentication, image validation, manifest parsing and anti-rollback checks.
- Validated **secure boot** and attestation across **10+ scenarios** using SHA hashing and **ECDSA verification** with mbedTLS.

Indian Institute of Technology Bombay, Edhaa Innovations *May 2025 – Jul 2025*

Electrical Intern *Mumbai, India*

- Designed and prototyped a **multi-slot bio-incubator** and **BioCheq device**, covering PCB design, BOM selection, STM32 and ESP32 I/O, sensors, power regulation, soldering, wiring and bring-up.
- Implemented embedded C firmware for sensor acquisition, **GPIO expansion and slot-level control**, increasing controllable channel capacity by **~60%** using shift registers.

Exegesis Infotech India Pvt Ltd. *May 2023 – Jul 2023*

Embedded Systems Intern *Navi Mumbai, India*

- Implemented embedded C routines for GPIO sequencing, peripheral initialization, timing-driven control logic and serial communication, **validating 90%+** of assigned interface test cases during board-level debugging.

PROJECTS

RISC-V SoC with AXI4 DMA and UVM Verification | SystemVerilog, UVM, SVA, AXI4, QuestaSim | **GitHub**

- Integrated a minimal RISC-V SoC with CPU-to-AXI adapter, **2-master and 2-slave AXI4 interconnect**, burst DMA, AXI SRAM, DMA register slave, reset handling and top-level integration.
- Implemented **memory-mapped AXI4 CPU-controlled DMA** with SRC_ADDR, DST_ADDR, LENGTH, CONTROL and STATUS registers, supporting **16-beat INCR bursts**, arbitration, backpressure, address decoding and response routing.
- Built a **UVM AXI verification environment** with sequences, drivers, monitors, scoreboards, protocol SVA, functional coverage, constrained-random tests and regression scripts across **4 DMA scenarios**.

2-Way Cache Memory Subsystem RTL with SECDED ECC and MBIST | SystemVerilog, SVA, QuestaSim | **GitHub**

- Designed a **512B, 2-way set-associative cache** with 16B lines, pseudo-LRU, write-back policy, dirty eviction and backing memory.
- Verified and debugged hits/misses, dirty eviction, ECC fault-injection and MBIST behavior using directed tests, **500 randomized transactions**, protocol assertions, reference-model scoreboarding, waveform debug, regression logs and **82%+ coverage.**
- Implemented **SECDED fault injection** and **March C-minus MBIST** with fail-address and data capture for DFT-oriented verification.

FPGA UART IP Core with FIFOs and Timing Closure | Vivado, Intel Quartus, SVA, Artix-7, Cyclone V | **GitHub**

- Designed UART IP with TX/RX datapaths, **8N1 framing, 16x oversampling**, configurable baud, FIFOs, loopback and register interface.
- Verified functionality using SVA, scoreboards, directed and randomized tests, FIFO stress, frame-error injection and overrun injection.
- Implemented RTL on Xilinx **Artix-7** and Intel **Cyclone V**, validating cross-vendor portability; met 100 MHz timing with **+5.318 ns** Vivado WNS, **+4.215 ns** Quartus setup slack and **234 LUTs, 489 FFs** on Artix-7.

EDUCATION

Birla Institute of Technology and Science, Pilani, India *Aug 2022 – Jul 2026*

Bachelor of Technology in Electrical and Electronics Engineering

Relevant Coursework: Digital Design, Analog and Digital VLSI Design, Microprocessors and Interfacing, Electronic Devices, Analog Electronics, Internet of Things, Control Systems, Microelectronic Circuits

TECHNICAL SKILLS

Languages: SystemVerilog, Verilog, C, C++, Python, Tcl

FPGA Design: FSMs, FIFOs, register interfaces, cache controllers, SECDED ECC, MBIST, Clock Domain Crossing, Static Timing Analysis

Verification: UVM, SVA, functional coverage, scoreboards, constrained-random testing, waveform debug, bounded proofs

Protocols: AMBA AXI4, AXI4-Lite, UART, SPI, I2C, memory-mapped interfaces, APB/AHB fundamentals

Tools/Software: QuestaSim, ModelSim, Xilinx Vivado, Intel Quartus, GTKWave, EasyEDA, LTspice, Altium Designer, SymbiYosys, Yosys, SMTBMC, Git, MATLAB, KiCad, Simulink, Arduino